# Shri Lemdeo Patil Mahavidyalaya

**Subject – Physics**

**Semester-VI**

**Topic- Operational Amplifier**

**By**

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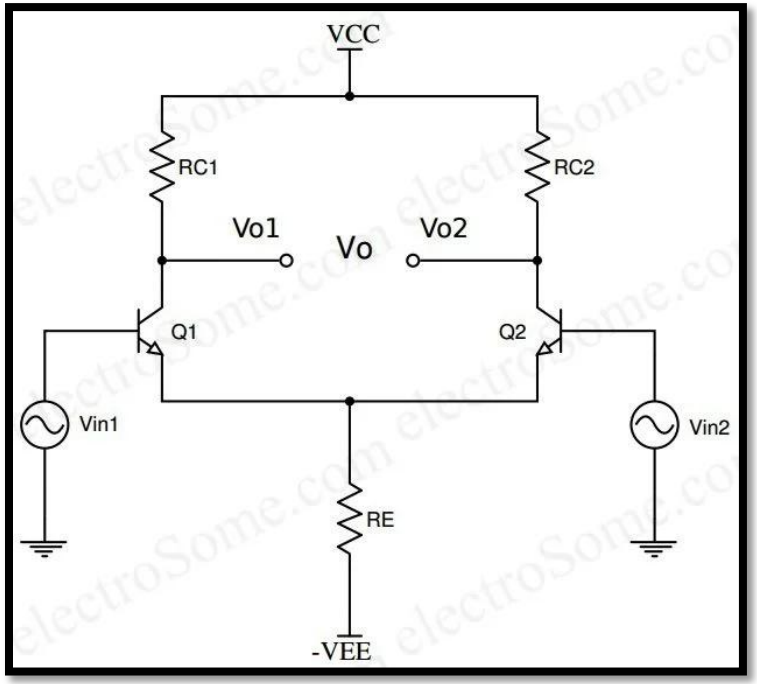
# Op-Amp

- It is DC coupled high gain voltage amplifier with differential input and single ended output
- It perform mathematical operations like Addition, Subtraction, Integration and Differentiation.
- The difference amplifier is a basic building block of OP-AMP.

# Differential Amplifier




- It amplify the **difference between two input signal**
- If **common mode signal** (equal in magnitude & in phase) is applied to both inputs then change in collector current of Q1 and Q2 will be identical and output voltage between two collector will be zero
- If **difference mode signal** is applied

$V_1 = -V_2$ (magnitude same but out of phase)

$\text{Gain} = V_o/V_i$

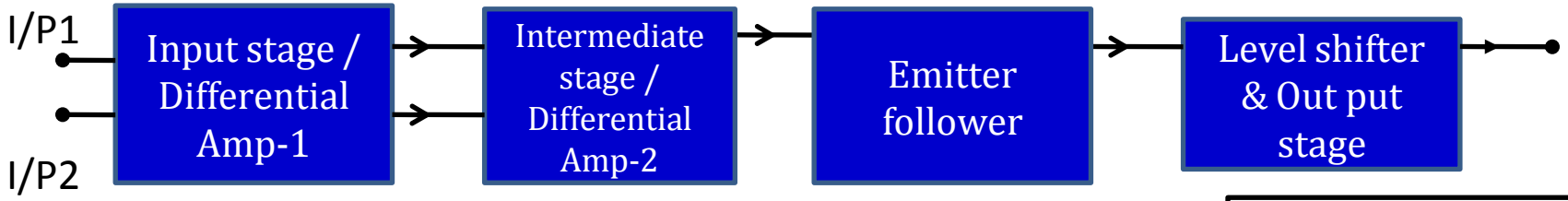
$= V_o/[V_1-(V_2)] = = V_o/[V_1-(-V_1)]$

$= V_o/2V_1$

$V_o = \text{Gain} \times 2V_1$

$V_1 = +5, V_2 = -5 \rightarrow V_o = \text{Gain} \times 2V_1 = \text{Gain} \times 2(5)$

# Block Diagram of an Op-AMP




**Input stage:-**

- two I/P & two O/P
- It posses large CMMR
- It helps to reduce noise
- I/P impedance is high
- It provide most of the voltage gain

**Intermediate stage:-**

- O/P of 1st stage is fed to intermediate stage
- It is multistage amplifier
- It provide large CMMR & large voltage gain

**Emitter Follower:-**

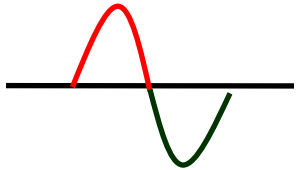
- It is an amplifier which has high I/P impedance & low O/P impedance
- Its gain is one (unity)
- It act as buffer between 2nd and 4th stage
- Avoid loading

**Level shifter:-**

- In the absence of any I/P, it brings O/P to zero level (ground potential)

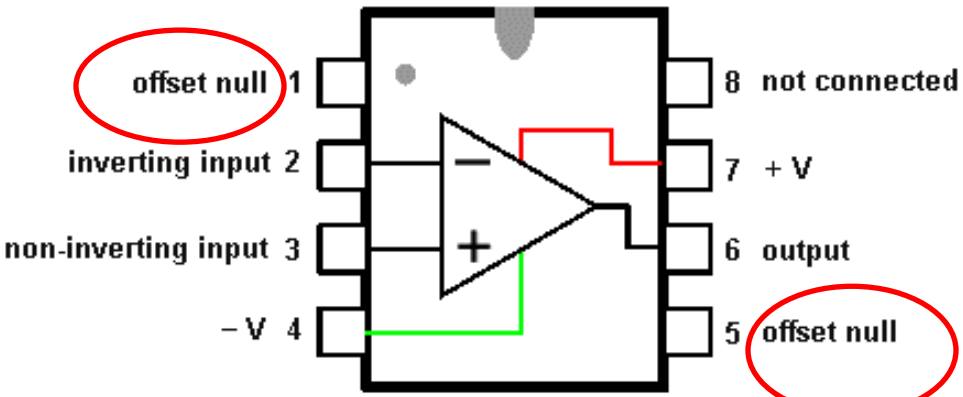
**Output stage:-**

- It is a push pull amplifier (two transistor are used in alternate half cycle of I/P signal



# 741

8-pin DIL (Dual In Line)




| Parameter | Symbol | Ideal Op-Amp | Practical Op-Amp |
|---|---|---|---|
| DC Open loop gain | $A_{OL}$ | ∞ | 100 dB |
| Input Impedance | $Z_{IN}$ | ∞ | 2MΩ |
| Output Impedance | $Z_{out}$ | 0 | 75Ω |
| Input Offset Voltage | $V_{IO}$ | 0 | 1mV |
| Slew rate | SR | ∞ | Depends on input signal frequency |
| Bandwidth | BW | ∞ | Depends on input signal frequency |
| CMRR | ρ | ∞ | 90 dB |

- **Slew rate:-** rate of change of output voltage with time.

- **Input bias current**:- the average value of current flow into each of the input terminals, when OPAMP is balanced.

- **CMMR**:- It is the ability of amplifier to reject common mode signal

$$CMMR = \frac{Differential\ mode\ gain}{common\ mode\ gain}$$